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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,225	11/17/2003	Arun Kwangil Iyengar	YOR920030488US1 (163-16)	5015

24336 7590 04/11/2008

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EXAMINER	
TSAI, SHENG JEN	

ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
04/11/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/715,225	**Applicant(s)** IYENGAR ET AL.	
	Examiner SHENG-JEN TSAI	**Art Unit** 2186	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 17 March 2008 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: _____.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: see below.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186

/Sheng-Jen Tsai/
PSA Examiner, Art Unit 2186

(1) Applicants contend that claims 1, 10-11 and 17-18 are patentable over Iyengar in view of Hiraoka, because the references fail to teach the limitation "delay an updating of the object until it is determined that each storage element instructed to invalidate a copy of the object has either (i) acknowledged that it is not storing a valid copy of the object or (ii) been deemed unresponsive." The Examiner disagrees.

First, Iyengar teaches that [In order to update a cache object, the central cache may communicate with the local caches to make sure that all copies are invalidated or updated (paragraph 0011)]. Thus the central cache delays the updating of an object until after it communicates communicate with the local caches to make sure that all copies are invalidated or updated.

Therefore, Iyengar at least implicitly alludes that the central cache delays the updating of an object until after it communicates communicate with the local caches to make sure that all copies are invalidated or updated.

Second, Hiraoka explicitly teaches a mechanism for coordinating invalidation (i.e., purging) of an object (i.e., the translation look-aside buffer) in which each of the storage element either acknowledges the invalidation of a copy of the object by sending back a "purge end signal" [A purge request source processor commonly supplies a purge request signal to other processors so as to cause them to perform TLB purge operations. A purge end signal sent back from other processors is stored in flip-flops in the source processor in units of processors. The source processor detects the end of TLB purge operations of all processors, in accordance with the statuses of the flip-flops (abstract); thus the acknowledgement from each storage element is stored and recorded in a corresponding flip-flop, and The source processor delays the updating until after it detects the end of TLB purge operations of all processors, in accordance with the statuses of the flip-flops], or is deemed unresponsible [The above operation can be performed when all the processors 200 through 203 are present. However, when the processor 203 is not present, the following operation is performed. The signal 483 representing that the processor 203 is not present is set at logic "1". The signal 483 of logic "1" is supplied to the OR gate 423. The OR gate 423 supplies the dummy TLB purge end signal to the AND gate 43. If the processor 203 is not present, the processor 200 can detect that all the TLB purge operations of the processors 200 through 202 are completed (column 4, lines 41-50). Note that processor 203 is the non-responsible element while processors 200 through 202 are responsive elements]

Therefore, Iyengar in view of Hiraoka clearly teaches the limitation recited in claims 1, 10-11 and 17-18.

(2) Applicants further contend that the teachings of Hiraoka regarding the process of purging Translation Look-aside Buffers (TLB) of a multiprocessor system are very much different and irrelevant to the systems and methods of the claimed inventions. The Examiner disagrees.

It should be noted that the limitation in question recites "delay an updating of the object until it is determined that each storage element instructed to invalidate a copy of the object has either (i) acknowledged that it is not storing a valid copy of the object or (ii) been deemed unresponsive."

Here the core of the event is "to invalidate a copy of the object." The Examiner explained earlier that the corresponding aspect in Hiraoka's invention "to invalidate a copy of the object" is "to purge a local copy of the TLB." Note that "a TLB" certainly qualifies as "an object," and that "purging a TLB" would actually "invalidate the TLB."

Therefore, Hiraoka's teachings of "purging a TLB" is directly related to the limitation "to invalidate a copy of the object" as recited in the claims.

(3) Therefore, the Examiner's position regarding the patentability of all claims remains the same as stated in the previous Office Action.